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PATENT APPLICATION

Applicant: Alain Blanc et al.
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Title:
QUEUE SCHEDULING MECHANISM IN A DATA PACKET TRANSMISSION SYSTEM

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Sir:

Applicants are hereby submitting certified copy of the foreign application, QUEUE SCHEDULING MECHANISM IN A DATA PACKET TRANSMISSION SYSTEM, Patent Application # 01480118.7 filed on 23 NOV 2001, as specified in 35 U.S.C. § 119(b).

Respectfully submitted,

Date: 28 August 2006

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

01480118.7

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Application no.: 01480118.7
Demande n°:

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Date of filing: 23/11/01
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Anmelder:
Applicant(s):
Demandeur(s):
INTERNATIONAL BUSINESS MACHINES CORPORATION
Armonk, NY 10504
UNITED STATES OF AMERICA

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Queue scheduling mechanism in a packet transmission system

In Anspruch genommene Prioriät(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

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QUEUE SCHEDULING MECHANISM IN A PACKET TRANSMISSION SYSTEM

Technical field

The present invention relates to the packet transmission systems wherein the data packets are transmitted from an input device to an output device through a switch engine and relates in particular to a queue scheduling mechanism in such a packet transmission system.

Background

In today's world of telecommunications, characterized by an insatiable demand for bandwidth, there are two particularly very fast growing technology sectors. These are, on one hand, the Internet and, on the second hand, wireless communications. If the first one is primarily concerned with data moving, the second is still mainly dealing with voice, so are the traditional phone carrier service providers. However, all of this is changing very rapidly. Service providers of all types tend to offer more services in an attempt to become, or to

stay, profitable. Service offerings range from long distance transport of voice and data over high-speed data backbone to the Internet and data services being offered on wireless pieces of equipment especially wireless phones of second and third generations.

If voice has long been transported under the form of data still, this is on circuit-switched TDM networks which are very different from the Internet packet networks obeying the Internet Protocol (IP). The former is a connection oriented network while the latter is connectionless. Hence, if the first one can offer the carrier-grade type of service required by delay-sensitive applications, such as voice, the second is just of a best effort kind however, well adapted to the transport of data.

All specialized transport network operators want to converge to a same "one-fits-all" type of network i.e. a packet network able to process differently flows of data depending on Quality of Service (QoS) schemes so as flows are indeed processed according to some specific requirements such as delay, jitter, bandwidth, and packet loss.

Switching and routing have been opposed for long in the manner the packets flow through the nodes of the network. The first one tightly associated to connection oriented protocols like ATM requires that a path be established prior to any data movement while routing is essentially the mode of operation of IP, and its hop-by-hop moving of data packets, with a decision to be made at each node. However, the end result is that whichever access protocol is in use, the networks are in actuality becoming switched-packet networks.

When packets arrive in a node, the layer 2 forwarding component of the switching node searches a forwarding table to make a routing decision for each packet. Specifically, the

forwarding component examines information contained in the packet's header, searches the forwarding table for a match, and directs the packet from the input interface to the output interface across the switch engine.

A switching node includes generally a plurality of output queues corresponding respectively to the plurality of output adapters and a shared memory for temporarily storing the incoming packets to be switched. The switch architecture is known to potentially provide the best possible performance allowing a full outgoing throughput utilization with no internal blocking and minimum delay.

Every queue is also organized by priority. That is, incoming packet headers, which carry a priority tag, are inspected not only to temporarily store packets in different queues, according to the output ports they are due to leave the switch engine but also are sorted by priority within each queue so that higher priority packets are guaranteed to be admitted first in the shared memory, getting precedence over lower priority traffic. In turn, the switch engine applies the same rule to the admitted packets, always privileging higher priorities. This is achieved by organizing the output queues by priority too. Hence, packet pointers, in each output queues are sorted so that admitted packets of higher priorities exit the switch engine first even though older packets, yet of a lower priority, are still waiting.

The priorities associated with the data packets are fully preemptive. Thus, if there are 4 priorities from P_0 to P_3, priority P_0 is going to take immediately precedence over any other traffic at priorities P_1-P_3 and so on. This is definitively a feature necessary to be able to handle a mix of voice and real-time traffic along with "pure" data traffic over a single network. This guarantees that data for the former type of applications are handled with no delay so that

there is no latency other than the necessary minimum time to traverse the switch engine and, even more importantly, in order that no significant jitter be added to any flow of real-time packets. However, this is necessarily done at the expense of lower priority traffic which has, in case of congestion, to wait. Even if this is not a problem since the transfer of data files is normally insensitive to delay and jitter, a lower priority e.g. P_3 may be completely starved by higher priorities e.g. P_0-P_2.

Summary of the invention

Accordingly, the main object of the invention is to provide a queue scheduling mechanism which avoids a lower priority from being prevented to transmit by higher priorities.

Another object of the invention is to provide a queue scheduling mechanism wherein a credit means enables to give a minimum bandwidth to the lower priority traffics.

The invention relates therefore to a queue scheduling mechanism in a packet transmission system comprising at least a transmission device for transmitting data packets, a reception device for receiving the data packets, a set of queue devices respectively associated with a set of priorities each defined by a priority rank for storing each data packet transmitted by the transmission device into the queue device corresponding to its priority rank, and a queue scheduler for reading, at each packet cycle, a packet in one of the queue devices determined by a normal priority preemption algorithm. This mechanism comprises a credit means providing, at each packet cycle, a value N defining the priority rank to be considered by the queue scheduler whereby a data packet is read by the queue scheduler from the queue device corresponding to the priority N instead of the queue device determined by the normal priority preemption algorithm.

Brief description of the drawings

The above and other objects, features and advantages of the invention will be better understood by reading the following more particular description of the invention in conjunction with the accompanying drawings wherein :

- Fig. 1 is a block-diagram representing schematically a switch device wherein a queue scheduling mechanism according to the invention is implemented.
- Fig. 2 is a flow chart representing the steps of the method implemented in the queue scheduling mechanism according to the invention.

Detailed description of the invention

The queue scheduling mechanism according to the invention is, in a preferred embodiment, implemented in a switch engine of a switching node wherein data packets are received from a plurality of input adapters and sent through the switch engine to another plurality of output adapters. However, such a mechanism could be used in any system wherein data packets received from transmitting devices are stored in queues according to several priorities before being read under the control of a queue scheduling mechanism for being sent to receiving devices.

Referring to Fig. 1, a switch engine 10 wherein the invention is implemented, comprises several queue devices 12, 14, 16 and 18 generally organized as FIFOs respectively associated with priority ranks P_0, P_1, P_2 and P_3. This means that data packets having a priority P_0 are stored in queue device 12, data packets of priority P_1 in queue device 14, data packets in priority P_2 in queue device 16, and data packets of priority P_3 in queue device 18.

At each packet cycle, the queue devices 12, 14, 16 and 18 have to be scheduled by a queue scheduler 20 through control lines 21 to allow a data packet to be read and sent to an output adapter 22 wherein the packet is stored in a queue device 24. However, a data packet may be read from a queue device of the switch engine 10 only if a GRANT signal sent on line 26 from the queue device 24 to the queue scheduler 20 is active. The activation of the grant signal for a given priority depends upon an algorithm which is a function of the filling level of queue device 24. Generally, there are several filling thresholds associated respectively with the priority ranks which make the GRANT signal inactive for a priority rank when the threshold associated with this priority rank is reached. Note that a packet of a priority N is read from the corresponding queue device 12, 14, 16 or 18 only if there is at least one packet stored in this queue device. The queue scheduler 20 is aware of this by means of lines 25 from the queue devices.

But the drawback of the system just described above is that a data packet having a low priority could stay in the switch engine for a very long time due to highest priority traffic resulting in holding a switch resource preventing highest priority packets to be queued and setting a time out at the end user level followed by a retransmission of the packet which increases the network congestion.

It is why the switch engine is also provided with a credit table 28 which enables to guarantee a minimum bandwidth for any priority rank. The credit table 28 which is programmable indicates which priority is allowed to be served unconditionally at each packet cycle, thus overriding the normal preemptive priority mechanism. Such a credit table can be a RAM memory having 256 locations wherein the address to be read is incremented at each packet cycle, the address

returning to 0 when it reaches the value 255. For example, the credit table can be organized in the following way :

Address	Priority
0	P3
1	P2
2	P1
:	:
12	P1
:	:
21	P2
22	P1
:	:
32	P1
:	:
41	P2
42	P1
:	:
100	P3
:	:

The number of location containing each value N is defined according to a predetermined percentage of occurrences with respect to the values of the other priority ranks. In the present case, it can be seen that the priority P_3 is registered at addresses 0, 100... that is in 1 location out of 100 locations of the credit table, the priority P_2 is registered at addresses 1, 21, 41, ... that is in 1 location out of 20 locations of the credit table and the priority P_1 is registered at addresses 2, 12, 22 ... that is 1 location out of 10 locations of the credit table, the other address locations being not fulfilled meaning the priority P_0 by default since,

in such a case, it is the priority P_0 which is served first before the other priorities.

Accordingly, the credit provided to the different priority ranks is the following in percentage :

P0	84%
P1	10%
P2	5%
P3	1%

The method for implementing the queue scheduling mechanism according to the invention is illustrated by the flow chart of Fig. 2. At each packet cycle, the credit table is first read (step 30) to know the priority N which is recorded at the address being read at this cycle, N being a number different from 0 as mentioned above or 0 by default. It is then checked whether the GRANT signal is active for this priority or, in other words, whether there is authorization to send a priority N packet (step 32). If so, it is determined whether there is a packet to be read in the queue corresponding to priority N (step 34). If it is the case, a priority N packet is read in the corresponding queue and sent to the output device (step 36). Then, the address of the credit table is incremented (step 38) and the process is looped back to step 30.

If the signal GRANT is not active for the priority N which has been read from the credit table or if there is no priority N packet in the corresponding queue, a variable n corresponding to the priority rank is set to 0 (step 40). It is then checked whether the GRANT signal is on (there is authorization to send a priority n packet) for the considered priority (step 42), that is the highest priority P_0 with n = 0. If so, it is determined whether there is a packet to be read in the queue corresponding to the priority n (step 44). If it is the case, a priority n packet is read from the queue corresponding to

this priority and sent to the output device (step 46). Then, the address of the credit table is incremented (step 38) and the process is looped back to step 30.

If the signal GRANT is not active for the priority n or if there is no priority n packet in the corresponding queue, it is checked whether the value of n has reached the value M corresponding to the lowest priority (step 48). If so, the address of the credit table is incremented and the process is looped back to step 30. If it is not the case, variable n is incremented to n + 1 (step 50) and the process returns to step 42 of processing the packet of priority n + 1, and so on.

It must be noted that, if there is a credit table in the switch engine and not in the input adapter and the output adapter, there is a risk that the lower priority packets be not scheduled and stay in the adapter queue as long as there is higher priority traffic. It is therefore necessary that a credit table with the same percentage of the priority ranks (e.g. 1% for P_3, 5% for P_2 and 10% for P_1 as seen above) exists in the input adapter as well as in the output adapter.

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CLAIMS

1. Queue scheduling mechanism in a packet transmission system comprising at least a transmission device for transmitting data packets, a reception device (22) for receiving said data packets, a set of queue devices (12, 14, 16, 18) respectively associated with a set of priorities each defined by a priority rank for storing each data packet transmitted by said transmission device into the queue device corresponding to its priority rank and a queue scheduler (20) for reading, at each packet cycle, a packet in one of said queue devices determined by a normal priority preemption algorithm;

   said mechanism being characterized in that it comprises a credit means (28) providing, at each packet cycle, a value N defining the priority rank to be considered by said queue scheduler whereby a data packet is read by said queue scheduler from the queue device corresponding to the priority N instead of said queue device determined by the normal priority preemption algorithm.

2. Queue scheduling mechanism according to claim 1, wherein said credit means is a credit table (28) storing at each address a value N equal to one of said priority ranks, the address to be read by said queue scheduler (20) for determining said priority N being incremented at each packet cycle after a data packet has been read from the queue device 12, 14, 16 or 18 corresponding to said priority N.

3. Queue scheduling mechanism according to claim 2, wherein a data packet is read by said queue scheduler (20) from said queue device (12, 14, 16 or 18) corresponding to said priority N only if an active GRANT signal from said reception device (22) is received by said queue scheduler.

4. Queue scheduling mechanism according to claim 3, wherein said GRANT signal depends upon the filling level of a receiving queue device (24) in said reception device (22) into which the data packets read from said queue devices (12, 14, 16 or 18) are stored.

5. Queue scheduling mechanism according to claim 4, wherein a data packet is read from the queue device (12, 14, 16, 18) determined by said normal priority preemption algorithm when there is no data packet available in the queue device corresponding to said priority N.

6. Queue scheduling mechanism according to claim 5, wherein the number of locations of said credit table (28) containing each value N is defined according to a predetermined percentage of occurrences with respect to the values of the other priority ranks.

7. Queue scheduling mechanism according to claim 6, wherein a number of locations in said credit table (28) contain no value meaning that the priority rank to be considered is the highest priority rank.

8. Queue scheduling mechanism according to any one of claimS 1 to 7, being used in a switch engine of a switching node within a network wherein said transmission device is an input adapter and said reception device is an output adapter.

QUEUE SCHEDULING MECHANISM IN A PACKET TRANSMISSION SYSTEM

Abstract

Queue scheduling mechanism in a packet transmission system comprising at least a transmission device for transmitting data packets, a reception device (22) for receiving the data packets, a set of queue devices (12, 14, 16, 18) respectively associated with a set of priorities each defined by a priority rank for storing each data packet transmitted by the transmission device into the queue device corresponding to its priority rank and a queue scheduler (20) for reading, at each packet cycle, a packet in one of the queue devices determined by a normal priority preemption algorithm. This mechanism comprises a credit means (28) providing, at each packet cycle, a value N defining the priority rank to be considered by the queue scheduler whereby a data packet is read by the queue scheduler from the queue device corresponding to the priority N instead of the queue device determined by the normal priority preemption algorithm.

FIG. 1

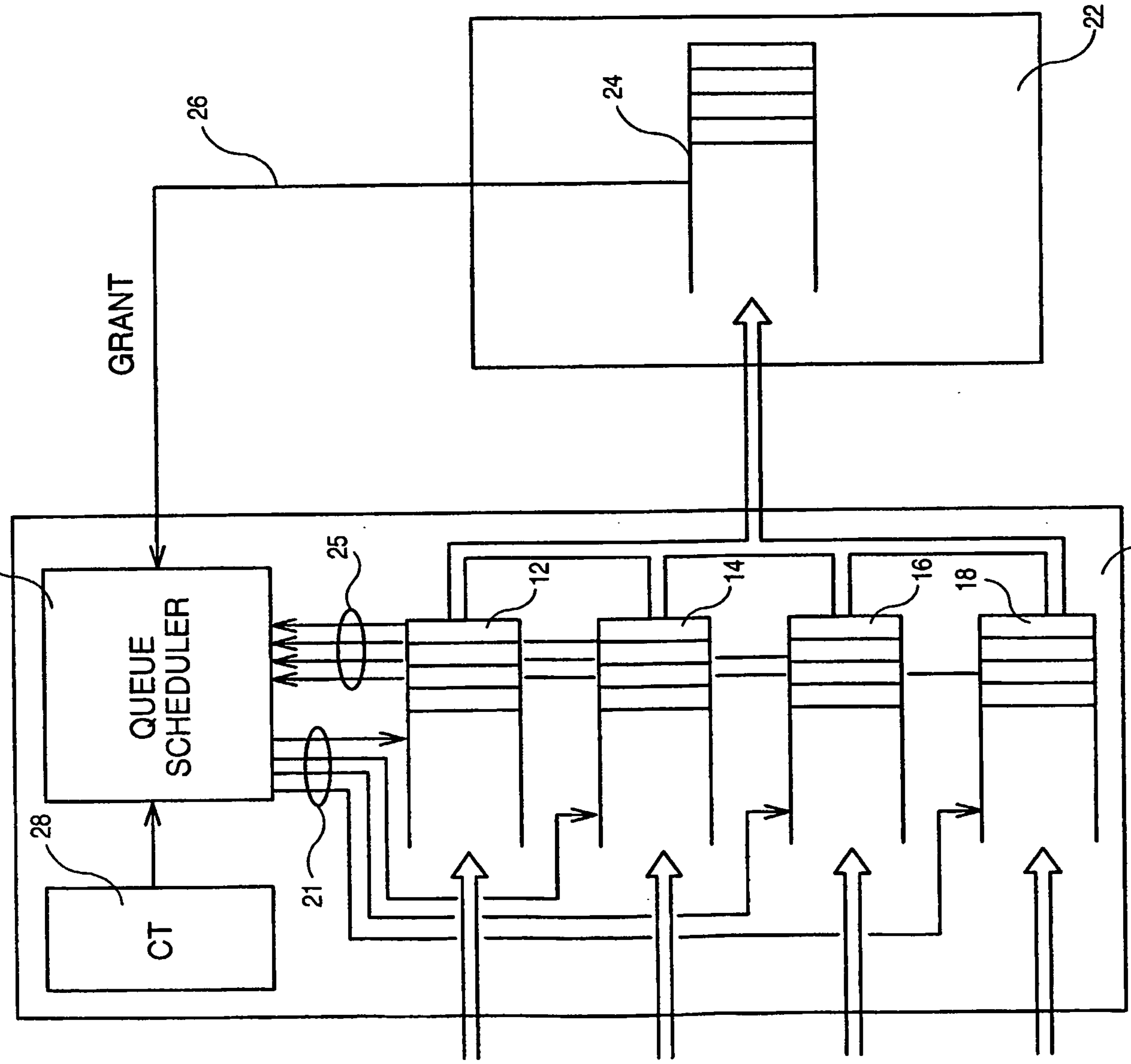

FIG. 1

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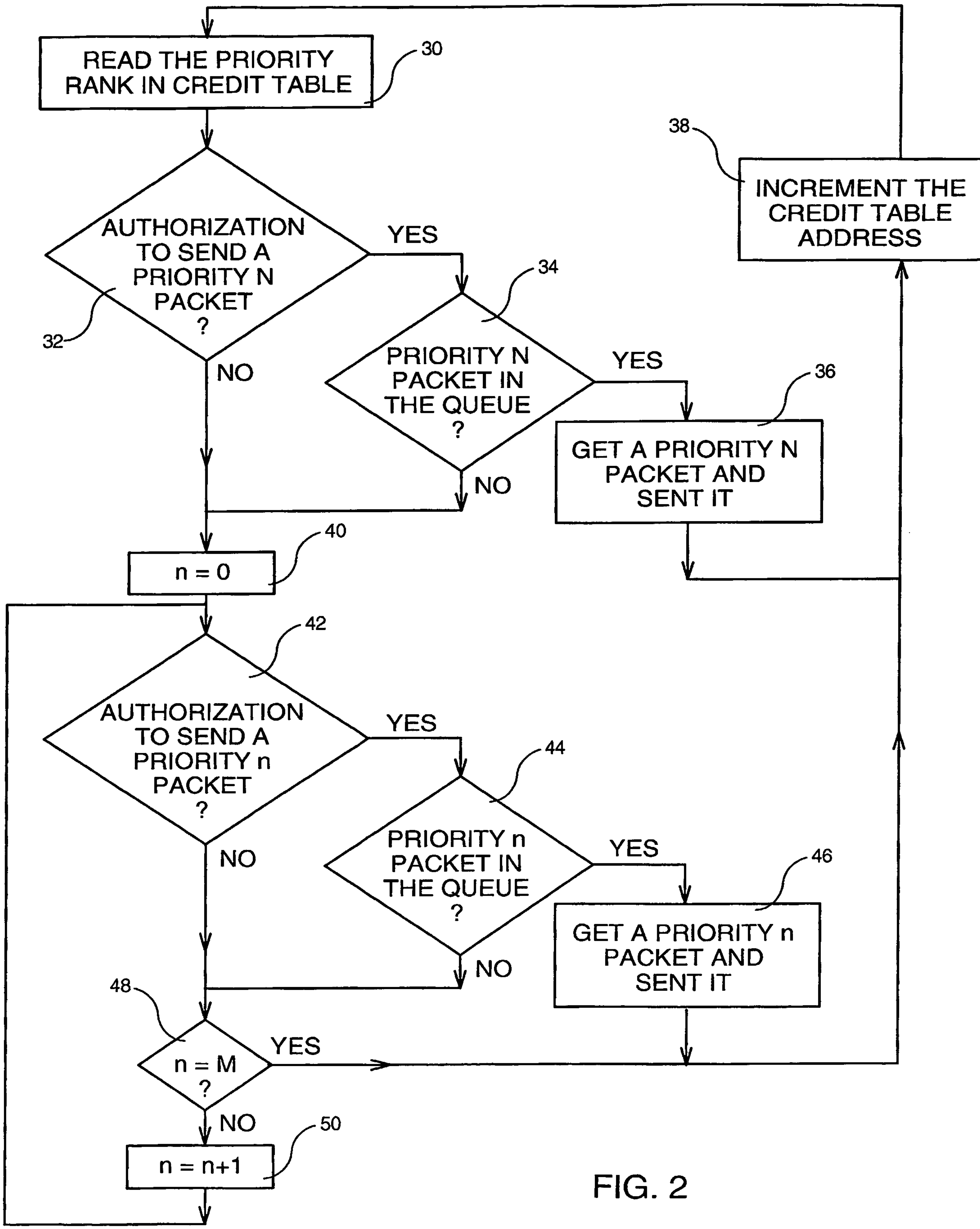

FIG. 2